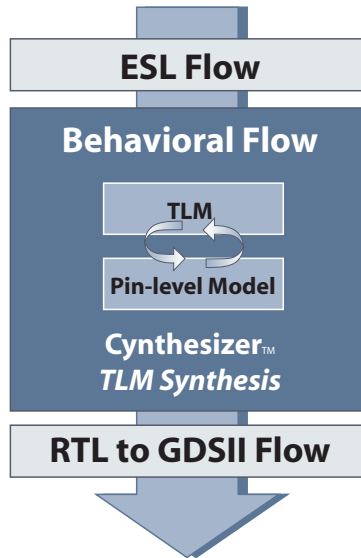


# Cynthesizer™ - TLM Synthesis

Accelerating ESL design to block-level implementation



*Cynthesizer's TLM Synthesis brings the industry's first integration of the ESL flow for system design with block-level implementation. With its unique approach to transaction-level model (TLM) design, TLM Synthesis provides a platform that unifies system architects, software developers, and hardware block designers.*

*Cynthesizer's TLM Synthesis allows a single source to be used, maintaining functional consistency throughout the ESL-to-GDSII implementation and verification process. As a result, you will be able to accelerate architecture exploration, achieve increased simulation performance and functional coverage, and minimize errors, leading to reduced design cost and faster time-to-market.*

## Completing the Integrated ESL-to-GDSII flow

TLM Synthesis allows transaction-level descriptions to be the link between TLM system-level design and the block-level implementation flow. As a result, system architects can leverage their existing SystemC TLM design methods, and block designers can use Cynthesizer in conjunction with their existing RTL-to-GDSII flows. Cynthesizer's TLM Synthesis option combined with its modular interface capability provides the cornerstone technology that supports an integrated ESL-to-GDSII design flow. This manages the complexities between system- and block-level design by allowing you to retain the consistency of your modeling efforts.

The system design process starts at the transaction level to define the overall architecture. These models are quick to build and fast to simulate because they do not contain implementation details. The block-level design process may start with the same transaction-level models. Once appropriate pin-level interfaces are selected, Forte's TLM Synthesis can create optimized RTL implementations while maintaining the transaction-level organization of the source code. High-speed TLM simulation at the block-level produces quicker verification and greater functional coverage.

The SystemC foundation of Cynthesizer accommodates integration with any TLM API and methodology, making Cynthesizer easier to deploy with your chosen TLM methodology.

### FEATURES

- Automatically switches between TLM and pin-level interfaces
- Allows use of sc\_port for abstract communication between modules
- Supports integration of Cynthesizer with any TLM environment
- Enables swapping of interfaces with different properties and characteristics
- Includes TLM versions of behavioral IP for fifos, memory interfaces, and streaming interfaces

### BENEFITS

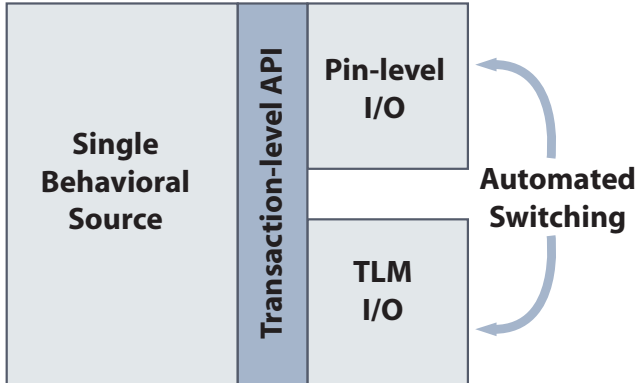
- Significantly increases simulation performance by raising abstraction level
- Integrates ESL and hardware implementation flows
- Permits early evaluation of system communication options
- Reduces effort by eliminating redundant model development
- Simplifies block implementation choice in the context of system architecture
- Provides foundation for complex behavioral IP reuse.

## Maintaining Model Consistency

TLM Synthesis maintains model consistency by using common behavioral source code for transaction-level simulation, pin-level behavioral simulation, and behavioral synthesis. Common behavioral source can be used for system and block-level design and verification tasks. You may define a set of functions that make up a transaction-level API for I/O communication. The behavior is then written using this transaction-level API. TLM Synthesis automatically switches between TLM interfaces and pin-level interfaces depending on the simulation configuration.

Maintaining common behavioral source at the transaction level ensures that only the interface behavior changes. The transaction semantics remain the same using signal-level or abstract communication mechanisms.

TLM Synthesis makes it possible to eliminate costly, redundant model development and avoids errors caused by inconsistencies between system models and the final implementation.



## Synthesizing What You Verify

Using the same source code for both synthesis and behavioral verification gives you added confidence that the final implementation will meet your design requirements. TLM Synthesis enhances Cynthesizer's ability to use the same testbench for pin-level and RTL verification with the addition of transaction-level support. In using SystemC semantics, the effort you spend on transaction and pin-level verification ensures the desired behavior in the resulting RTL.

## Included Transaction-level IP

TLM Synthesis includes a transaction-level set of behavioral IP to accompany the pin-level set included with Cynthesizer:

- Fifos
- Memory interfaces
- Streaming interfaces
- OSCI TLM Library support

## Why is TLM important at the block level?

While TLM is widely used by system designers, block designers using Cynthesizer will greatly benefit in using TLM Synthesis. It facilitates high-speed TLM simulations for block-level verification, which reduces verification time or allows greater functional coverage in the time allocated for simulation.

Using transaction-level interfaces results in functional simulation 5X - 10X faster than pin-level behavioral simulation or 50X to 200X faster than RTL simulation. For 60% - 80% of all block-level behavioral simulation runs, TLM simulation may be used. The remainder requires the use of pin-level interfaces either to validate pin-level behavior or to simulate with other blocks using pin-level interfaces.

## FORTE DESIGN SYSTEMS

Forte Design Systems  
headquarters:  
100 Century Center Court  
Suite 100  
San Jose, CA 95112 USA  
tel: 408.432.9430  
fax: 408.432.9433  
email: sales@ForteDS.com

Forte Design Systems  
European office:  
tel:+33 468 940 808  
fax:+33 680 130 909  
email:fconstant@forteds.com

[www.ForteDS.com](http://www.ForteDS.com)