



NEWS RELEASE

Forte Design Systems Ships Latest Version of CellMath Designer Improvements Reduce Area, Increase Performance, Lower Power Consumption on Datapath-Intensive Design Blocks

SAN JOSE, CALIF. — March 5, 2010 — Forte Design Systems, a leading provider of SystemC high-level synthesis, datapath synthesis and intellectual property (IP), announced it is shipping the latest version of CellMath Designer datapath synthesis and CellMath IP software.

The CellMath family allows register-transfer level (RTL) designers to reduce area, improve performance and lower power consumption for their existing datapath-intensive design blocks.

"We're seeing strong demand to reduce power and area, and create more competitive designs in virtually all market segments," says Brett Cline, Forte's vice president of marketing and sales. "Design teams that added CellMath Designer and CellMath IP to their existing logic synthesis or high-level synthesis design flow have been able to obtain optimal results quickly and at low cost."

This version of CellMath Designer, the first release from Forte since it acquired Arithmatica in 2009, provides more automation to get users to optimal results with less effort. Other features include improved RTL code optimizations, a new bi-directional retiming algorithm and more scripting control, which mean that existing RTL designs can be used with no modifications.

For existing users, CellMath Designer's multiplexor synthesis capability has been extended. This will provide more optimal results when optimizing across many levels of multiplexors, including recognizing complex pipeline enable signals formed from multiple levels of logic to improve ease of use and overall quality of results (QoR).

Improved Formal Verification Flow for Datapath Designs

Traditionally, datapath blocks present unique challenges for formal verification tools because of the difficulty of comparing the original RTL input with the gate-level output after several complex transformations.

CellMath Designer's unique approach to formal verification has been further extended to provide even more power to users. In this release, users have complete control over which parts of their design are described in RTL code and which at the gate-level, along with control over which carry-save outputs include final additions. This enables users to break verification problems into a chain of simpler/smaller steps that formal verification software can manage. With these new features, unresolved verification tasks can be turned from "inconclusive" to "equivalent."

CellMath IP

CellMath Designer utilizes optimal, mathematically designed arithmetic operators and functions to improve overall quality of results in datapath-dominated designs. Together with CellMath Designer's datapath synthesis capabilities, designers find that utilizing CellMath IP operators improves overall QoR, especially power, on existing RTL designs.

CellMath IP includes patented arithmetic architectures for floating-point, fixed-point and integer-based designs, and is being used in millions of leading-edge devices around the world.

Availability and Pricing

The latest version of CellMath Designer is shipping now. U.S. pricing starts at \$120,000 for a one-year, time-based license.

About Forte Design Systems

Forte Design Systems is a leading provider of software products that enable design at a higher level of abstraction and improve design results. Its innovative synthesis technologies and intellectual property offerings allow design teams creating complex electronic chips and systems to reduce their overall design and verification time. More than half of the top 20 worldwide semiconductor companies use Forte's products in production today for ASIC, SoC and FPGA design. Forte is headquartered in San Jose, Calif., with additional offices in England, Japan, Korea, and the United States. For more information, visit www.ForteDS.com.

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