FORTE DESIGN SYSTEMS

Cellmath™ Designer

DATAPATH INTENSIVE APPLICATIONS

- Media processing
  - Graphics
  - Video
  - Audio
  - Imaging
  - Communications
- Network processing
  - Wireless
  - Wireline
- Cryptography
- High-performance computing
- Consumer electronics

HIGHLIGHTS

- Plug and Play Design Solution
  - Synopsys
  - Cadence
  - Magma
- Standards
  - Verilog inputs and outputs
  - Synopsys library format (.lib)
  - Synopsys design constraints (.sdc)
- Automatic gate-level optimization
  - Power, area, and/or speed
  - Auto-pipelining and retiming
- Eases simulation/formal verification flow
  - Bit-accurate C models
  - Hierarchical Verilog models
  - Formality and Conformal compliance
- Floating point functions
  - IEEE 754 formats
  - Configurable mantissa and exponent widths
  - Rounding
  - Internal guard-banding
  - Pipeline depth

OVERVIEW

CellMath Designer (CMD) is an innovative datapath synthesis tool that automatically creates high quality gate-level designs optimized for power, area, and timing. CMD easily integrates into your existing Cadence, Synopsys, or Magma IC design flow by utilizing industry standard tool interfaces and data formats. CMD reads standard Verilog RTL models extended with datapath pragmas and automatically produces an optimized Verilog gate-level netlist. CMD also produces bit-accurate C and hierarchical Verilog models to support your simulation and formal verification process respectively. Your target technology is installed via standard cell libraries in the Synopsys Liberty format (.lib). CMD reads your design constraints using the Synopsys Design Constraints (.sdc) format.

CMD enables IC designers to rapidly explore datapath design implementation alternatives prior to integration into their SOC design. CMD is built upon the industry's most advanced and comprehensive algorithms and heuristics for power, area and timing optimization of datapaths. CMD provides automatic partitioning of the datapath section of your RTL models, freeing your IC designers from the task of manually dissecting their designs. Using its RTL transformation technology, CMD then automatically creates an optimal internal representation of your RTL model for use in datapath synthesis. By successively applying algorithms for architectural selection, multiplexer synthesis, pipelining/retiming and logic optimization/mapping, CMD automatically produces the best gate-level implementation possible based on the design constraints you have specified.

Floating point functions can be called from your RTL model with associated parameters that specify precision, internal rounding, and control options. Floating point functions are synthesized from multiple potential micro-architectures to provide the designer with optimal power, area, and timing gate-level implementations. All floating point functions utilize the IEEE 754 bit format.

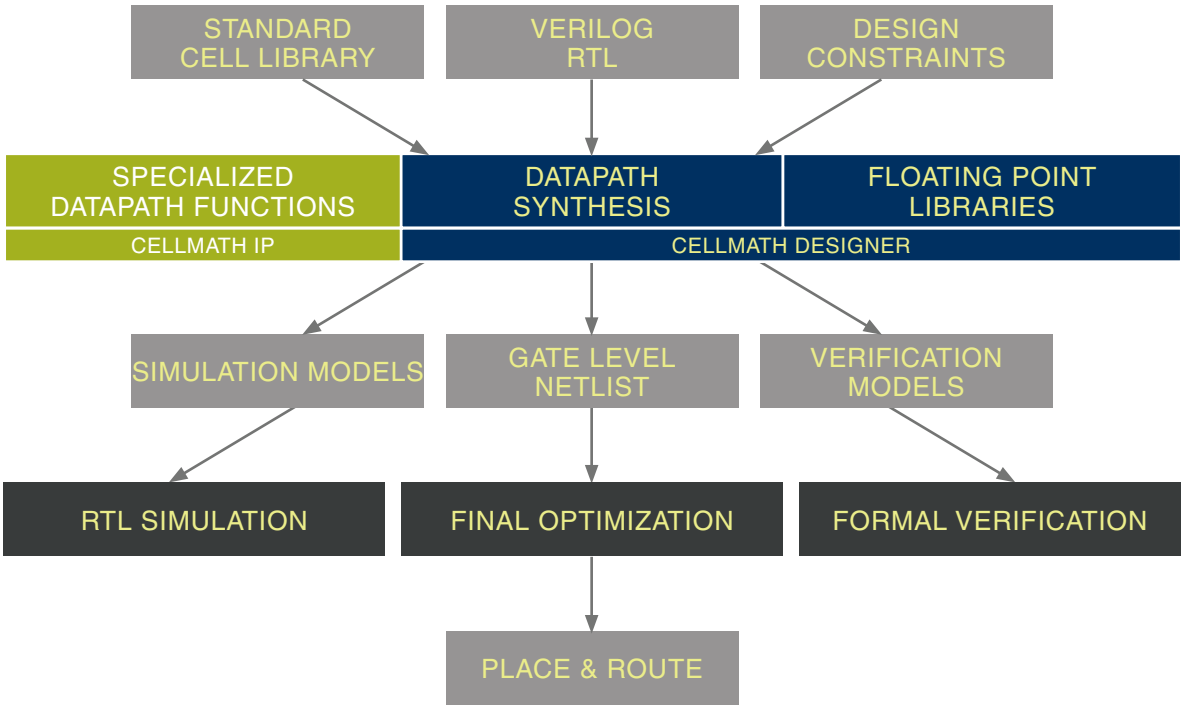
"ATI has deployed CellMath Designer for datapath design in our graphics production flow. We were able to achieve aggressive datapath area targets with a solution that integrated well with our current design flow."

Greg Buchner, VP of Engineering
ATI, a Division of AMD

"CellMath Designer enabled our team to significantly reduce overall chip power and reduce datapath area while meeting the throughput requirements in our critical signal processing blocks."

Sridhar Begur, Vice President, ASIC Engineering
Teranetics

CELLMATH DATAPATH DESIGN AUTOMATION FLOW



EDA ALLIANCES

Synopsys TAP-IN
Cadence Connections
Magma Ties

SYSTEM REQUIREMENTS

OPERATING SYSTEM
RedHat Version 7 or higher
RHE Version 2.4 or higher
Fedora Version 2 or higher

PROCESSOR
Minimum 1GHz; Recommended: 3GHz

MEMORY REQUIREMENTS
Minimum 500Mb; Recommended 2Gb

STORAGE REQUIREMENTS
Minimum 90Mb

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